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**BEST AVAILABLE COPY**In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

- 1 1. (Currently Amended) A signal interface, comprising:
  - 2 a set of signal lines having  $N+1$  signal lines, where  $N$  is an integer;
  - 3  $N+1$  receivers coupled to respective signal lines in the set of signal lines
  - 4 establishing a set of  $N+1$  signal paths with the set of signal lines;
  - 5 an  $N$  line bus;
  - 6 a line maintenance circuit; and
  - 7 a switch in the  $N+1$  signal paths, and control logic for the switch, which
  - 8 selectively routes  $N$  signal paths in the set to the  $N$  line bus and signal path ( $n$ ) in the set
  - 9 to the line maintenance circuit, where ( $n$ ) is changed according to a pattern to selectively
  - 10 maintain signal paths in the set of  $N+1$  signal paths while enabling data flow on  $N$  signal
  - 11 paths in the set to the  $N$  line bus; wherein for a change of (n) by switching a first
  - 12 particular signal path from routing to the line maintenance circuit to routing to a line in
  - 13 the N line bus, and a second particular signal path from routing to the line in the N line
  - 14 bus to the line maintenance circuit, the control logic controls the switch so that reception
  - 15 of data from the line in the N line bus is uninterrupted.
- 1 2. (Original) The signal interface of claim 1, wherein the pattern comprises a periodic
- 2 pattern.
- 1 3. (Original) The signal interface of claim 1, wherein the set of  $N+1$  signal paths
- 2 includes signal paths logically identified as paths 0 to  $N$ , and the pattern comprises a
- 3 repeating pattern beginning with ( $n$ ) equal to 0 and increasing to ( $n$ ) equal to  $N$ , and then
- 4 decreasing to ( $n$ ) equal to 0.
- 1 4. (Original) The signal interface of claim 1, wherein the receivers are responsive to
- 2 respective receive clock signals produced by adjustable clock generators, and said line
- 3 maintenance circuits set the adjustable clock generators.

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1 5. (Original) The signal interface of claim 1, wherein the receivers are responsive to  
2 respective receive clock signals produced by adjustable clock generators, and said line  
3 maintenance circuit sets the adjustable clock generators in response to a calibration data  
4 pattern on the signal path coupled to the line maintenance circuit.

1 6. (Currently Amended) A signal interface comprising:  
2 a set of signal lines having N+1 signal lines, where N is an integer;  
3 N+1 receivers coupled to respective signal lines in the set of signal lines  
4 establishing a set of N+1 signal paths with the set of signal lines;  
5 an N line bus;  
6 a line maintenance circuit; and  
7 a switch in the N+1 signal paths, and control logic for the switch, which  
8 selectively routes N signal paths in the set to the N line bus and signal path (n) in the set  
9 to the line maintenance circuit, where (n) is changed according to a pattern to selectively  
10 maintain signal paths in the set of N+1 signal paths while enabling data flow on N signal  
11 paths in the set to the N line bus The signal interface of claim 1, wherein the control logic  
12 controls the switch for a change of (n) by switching a first particular signal path from  
13 routing to the line maintenance circuit to routing to a line in the N line bus, and a second  
14 particular signal path from routing to the line in the N line bus to the line maintenance  
15 circuit, the control logic controls the switch so that during a settling interval, the first and  
16 second particular signal paths both carry data from are routed together to the line in the N  
17 line bus, and then after the settling interval the second particular signal path is coupled to  
18 the line maintenance circuit.

1 7. (Original) The signal interface of claim 1, wherein the control logic includes logic  
2 for coordinating the pattern with a source of data for the N line bus.

1 8. (Original) The signal interface of claim 1, wherein said N+1 receivers, said N line  
2 bus, said line maintenance circuit; and said switch comprise components of a single  
3 integrated circuit.

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1 9. (Original) The signal interface of claim 1, including logic to power down the N+1  
2 receivers while continuing to selectively maintain signal paths in the set of signal paths.

1 10. (Original) The signal interface of claim 1, wherein the N+1 receivers are adapted to  
2 receive data with a data rate higher than 100 MegaHertz.

1 11. (Original) The signal interface of claim 1, wherein said N+1 receivers, said N line  
2 bus, said line maintenance circuit; and said switch comprise components of a single  
3 integrated circuit, and the N+1 receivers are adapted to receive data with a data rate  
4 higher than 100 MegaHertz from a source external to the integrated circuit.

1 12. (Original) The signal interface of claim 1, further including an additional signal line  
2 adapted to receive a source synchronous clock.

1 13. (Currently Amended) A signal interface, comprising:  
2 an N line bus;  
3 a set of signal lines having N+1 signal lines, where N is an integer;  
4 N+1 transmitters coupled to respective signal lines in the set of signal lines;  
5 establishing a set of N+1 signal paths with the set of signal lines;  
6 a line maintenance circuit; and  
7 a switch in the N+1 signal paths, and control logic for the switch, which  
8 selectively routes N signal paths in the set from the N line bus to N signal lines in the set  
9 of signal lines, and routes signal path (n) in the set from the line maintenance circuit to  
10 signal line (n) in the set of signal lines, where (n) is changed according to a pattern to  
11 selectively perform maintenance on signal paths in the set of N+1 signal paths while  
12 enabling data flow on N signal paths in the set from the N line bus; wherein for a change  
13 of (n) by switching a first particular signal path from routing to the line maintenance  
14 circuit to routing to a line in the N line bus, and a second particular signal path from  
15 routing to the line in the N line bus to the line maintenance circuit, the control logic

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16 controls the switch so that transmission of data from the line in the N line bus is  
17 uninterrupted.

1 14. (Original) The signal interface of claim 13, wherein the pattern comprises a periodic  
2 pattern.

1 15. (Original) The signal interface of claim 13, wherein the set of N+1 signal paths  
2 includes signal paths logically identified as paths 0 to N, and the pattern comprises a  
3 repeating pattern beginning with (n) equal to 0 and increasing to (n) equal to N, and then  
4 decreasing to (n) equal to 0.

1 16. (Original) The signal interface of claim 13, wherein the line maintenance circuit  
2 comprises a calibration signal source that produces a signal pattern adapted for  
3 calibration of receive clock signals.

1 17. (Original) The signal interface of claim 13, wherein the line maintenance circuit  
2 comprises a calibration signal source that produces a pseudo random signal pattern  
3 adapted for calibration of receive clock signals.

1 18. (Currently Amended) A signal interface, comprising:  
2 an N line bus;  
3 a set of signal lines having N+1 signal lines, where N is an integer;  
4 N+1 transmitters coupled to respective signal lines in the set of signal lines  
5 establishing a set of N+1 signal paths with the set of signal lines;  
6 a line maintenance circuit; and  
7 a switch in the N+1 signal paths, and control logic for the switch, which  
8 selectively routes N signal paths in the set from the N line bus to N signal lines in the set  
9 of signal lines, and routes signal path (n) in the set from the line maintenance circuit to  
10 signal line (n) in the set of signal lines, where (n) is changed according to a pattern to  
11 selectively perform maintenance on signal paths in the set of N+1 signal paths while  
12 enabling data flow on N signal paths in the set from the N line bus. The signal interface

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13 of claim 13, wherein the control logic controls the switch for a change of (n) by switching  
14 a first particular signal path from routing from the line maintenance circuit to routing to a  
15 line in the N line bus, and a second particular signal path from routing to the line in the N  
16 line bus from the line maintenance circuit, the control logic controls the switch so that  
17 during a settling interval, the first and second particular signal paths both carry data are  
18 routed together to the line in the N line bus, and then after the settling interval the second  
19 particular signal path is coupled to the line maintenance circuit.

1 19. (Original) The signal interface of claim 13, wherein the control logic includes logic  
2 for coordinating the pattern with a destination of data for the N line bus.

1 20. (Original) The signal interface of claim 13, wherein said N+1 transmitters, said N  
2 line bus, said line maintenance circuit; and said switch comprise components of a single  
3 integrated circuit.

1 21. (Original) The signal interface of claim 13, including logic to power down the N+1  
2 transmitters while continuing to selectively perform maintenance on signal paths in the  
3 set of N+1 signal paths.

1 22. (Original) The signal interface of claim 13, wherein the N+1 transmitters are adapted  
2 to transmit data with a data rate higher than 100 MegaHertz.

1 23. (Original) The signal interface of claim 13, wherein said N+1 transmitters, said N  
2 line bus, said line maintenance circuit; and said switch comprise components of a single  
3 integrated circuit, and the N+1 transmitters are adapted to transmit data with a data rate  
4 higher than 100 MegaHertz to a destination external to the integrated circuit.

1 24. (Original) The signal interface of claim 13, further including an additional signal  
2 line adapted to transmit a source synchronous clock.

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1 25. (Currently Amended) A communication system for inter-chip signals,  
2 comprising:  
3 a first integrated circuit, a second integrated circuit, and a set of N+1  
4 communications lines between the first and second integrated circuits;  
5 the first integrated circuit comprising  
6 a first N line bus, where N is an integer;  
7 a set of transmitter signal lines having N+1 transmitter signal lines  
8 coupled to respective communications lines in the set of N+1 communications lines;  
9 N+1 transmitters coupled to respective transmitter signal lines in the set of  
10 transmitter signal lines establishing a set of N+1 transmitter signal paths with the set of  
11 transmitter signal lines;  
12 a calibration signal source; and  
13 a switch in the N+1 transmitter signal paths, and first control logic for the  
14 switch, which selectively routes N transmitter signal paths in the set from the first N line  
15 bus to N transmitter signal lines in the set of signal lines, and routes transmitter signal  
16 path (n) in the set from the calibration signal source to one transmitter signal line in the  
17 set of transmitter signal lines, where (n) is changed according to a pattern to selectively  
18 supply calibration signals on communication lines in the set of N+1 communication lines  
19 while enabling data flow on N communication lines in the set from the first N line bus;  
20 and  
21 the second integrated circuit comprising  
22 a set of receiver signal lines having N+1 receiver signal lines coupled to  
23 respective communications lines in the set of N+1 communications lines;  
24 N+1 receivers coupled to respective receiver signal lines in the set of  
25 receiver signal lines establishing a set of N+1 receiver signal paths with the set of  
26 receiver signal lines;  
27 a second N line bus;  
28 a calibration circuit; and  
29 a switch in the N+1 receiver signal paths, and second control logic for the  
30 switch, which selectively routes N receiver signal paths in the set to the second N line bus  
31 and receiver signal path (n) in the set to the calibration circuit, where (n) is changed

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32 according to the pattern to selectively calibrate receiver signal paths in the set of N+1  
33 receiver signal paths while enabling data flow on N receiver signal paths in the set to the  
34 second N line bus; and

35 control logic on at least one of the first and second integrated circuits; wherein for  
36 a change of (n) by switching a first particular signal path from routing between the  
37 calibration signal source and the calibration circuit to routing to between lines in the first  
38 and second N line buses, and a second particular signal path from routing between lines  
39 in the first and second N line buses to routing between the calibration signal source and  
40 the calibration circuit, the control logic controls the switch so that transmission of data  
41 from between the lines in the first and second N line buses is uninterrupted.

1 26. (Original) The communication system of claim 25, wherein the pattern comprises a  
2 periodic pattern.

1 27. (Original) The communication system of claim 25, wherein the set of N+1 receiver  
2 signal paths includes receiver signal paths logically identified as paths 0 to N, and the  
3 pattern comprises a repeating pattern beginning with (n) equal to 0 and increasing to (n)  
4 equal to N, and then decreasing to (n) equal to 0.

1 28. (Original) The communication system of claim 25, wherein the calibration signal  
2 source produces a signal pattern adapted for calibration of receive clock signals.

1 29. (Original) The communication system of claim 25, wherein the calibration signal  
2 source produces a pseudo random signal pattern adapted for calibration of receive clock  
3 signals.

1 30. (Currently Amended) A communication system for inter-chip signals.  
2 comprising:  
3 a first integrated circuit, a second integrated circuit, and a set of N+1  
4 communications lines between the first and second integrated circuits;  
5 the first integrated circuit comprising:

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6                   a first N line bus, where N is an integer;  
7                   a set of transmitter signal lines having N+1 transmitter signal lines  
8                   coupled to respective communications lines in the set of N+1 communications lines;  
9                   N+1 transmitters coupled to respective transmitter signal lines in the set of  
10                   transmitter signal lines establishing a set of N+1 transmitter signal paths with the set of  
11                   transmitter signal lines;  
12                   a calibration signal source; and  
13                   a switch in the N+1 transmitter signal paths, and first control logic for the  
14                   switch, which selectively routes N transmitter signal paths in the set from the first N line  
15                   bus to N transmitter signal lines in the set of signal lines, and routes transmitter signal  
16                   path (n) in the set from the calibration signal source to one transmitter signal line in the  
17                   set of transmitter signal lines, where (n) is changed according to a pattern to selectively  
18                   supply calibration signals on communication lines in the set of N+1 communication lines  
19                   while enabling data flow on N communication lines in the set from the first N line bus;  
20                   and  
21                   the second integrated circuit comprising:  
22                   a set of receiver signal lines having N+1 receiver signal lines coupled to  
23                   respective communications lines in the set of N+1 communications lines;  
24                   N+1 receivers coupled to respective receiver signal lines in the set of  
25                   receiver signal lines establishing a set of N+1 receiver signal paths with the set of  
26                   receiver signal lines;  
27                   a second N line bus;  
28                   a calibration circuit; and  
29                   a switch in the N+1 receiver signal paths, and second control logic for the  
30                   switch, which selectively routes N receiver signal paths in the set to the second N line bus  
31                   and receiver signal path (n) in the set to the calibration circuit, where (n) is changed  
32                   according to the pattern to selectively calibrate receiver signal paths in the set of N+1  
33                   receiver signal paths while enabling data flow on N receiver signal paths in the set to the  
34                   second N line bus; and  
35                   wherein The communication system of claim 25, wherein the first control logic  
36                   controls the switch for a change of (n) by switching a first particular transmitter signal

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37 path from routing from the calibration signal source to routing from a line in the first N  
38 line bus, and a second particular transmitter signal path from routing from the line in the  
39 first N line bus to routing from the calibration signal source, the first control logic  
40 controls the switch in the N+1 transmitter signal paths so that during a settling interval,  
41 the first and second particular transmitter signal paths both carry data are routed together  
42 from the line in the first N line bus, and then after the settling interval the second  
43 particular signal path is routed from the calibration signal source.

1 31. (Currently Amended) The communication system of claim 30 25, wherein the  
2 first control logic controls the switch for a change of (n) by switching a first particular  
3 receiver signal path from routing to the calibration circuit to routing to a line in the  
4 second N line bus, and a second particular receiver signal path from routing to the line in  
5 the second N line bus to the calibration circuit, the second control logic controls the  
6 switch in the N+1 receiver signal paths so that during a settling interval, the first and  
7 second particular receiver signal paths both carry data for are routed together to the line  
8 in the second N line bus, and then after the settling interval the second particular receiver  
9 signal path is coupled to the calibration circuit.

1 32. (Original) The communication system of claim 25, wherein the first control logic  
2 and second control logic include logic for coordinating the pattern.

1 33. (Original) The communication system of claim 25, including logic to power down  
2 the N+1 transmitters while continuing to selectively supply calibration signals on  
3 transmitter signal paths in the set of N+1 transmitter signal paths.

1 34. (Original) The communication system of claim 25, including logic to power down  
2 the N+1 receivers while continuing to selectively calibrate receiver signal paths in the set  
3 of N+1 receiver signal paths.

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1 35. (Original) The communication system of claim 25; wherein the N+1 transmitters and  
2 the N+1 receivers are adapted to communicate via the set of communications lines with a  
3 data rate higher than 100 MegaHertz.

1 36. (Original) The communication system of claim 25, further including an additional  
2 communication line adapted for a source synchronous clock.

1 37. (Original) A method for managing a high speed communication interface for a  
2 parallel bus having N bus lines, where N is an integer, comprising:  
3 establishing N+1 communication lines;  
4 performing a maintenance operation on communication line (n) of the N+1  
5 communications lines and enabling paths from the N bus lines on N of the N+1  
6 communications lines;  
7 after performing the maintenance operation on communication line (n) of the N+1  
8 communications lines, changing (n) and performing a maintenance operation a next  
9 communication line of the N+1 communication lines.

1 38. (Currently Amended) The method of claim 37, wherein performing the  
2 maintenance operation includes:  
3 transmitting a calibration signal on the communication line (n) from a calibration  
4 signal source;  
5 receiving the calibration signal on the communication line (n) of the N+1  
6 communications lines; and  
7 calibrating a parameter associated with the communication line (n) on the N+1  
8 communications lines in response to the calibration signal.

1 39. (Currently Amended) The method of claim 37, including transmitting data from  
2 the N bus lines while performing the maintenance operation on the communication line  
3 (n).

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1 40. (Currently Amended) The method of claim 37, including entering a reduced  
2 power consumption state on at least one of receivers and transmitters on the N of the  
3 communication lines, while performing the maintenance operation on the communication  
4 line (n).

1 41. (Original) The method of claim 37, for a changing (n) to switch a first particular  
2 communication line from subject of the maintenance operation to communicating from a  
3 line on the N line bus, and a second particular communication line from communicating  
4 from the line on the N line bus to subject of the maintenance operation, routing the first  
5 and second particular communication lines together from the line in the N line bus during  
6 a settling interval, and then after the settling interval performing the maintenance  
7 operation on the second particular communication line.

1 42. (Original) The method of claim 37, including changing (n) according to a continuous  
2 periodic pattern.

1 43. (Original) The method of claim 37, wherein the set of N+1 communication lines  
2 includes communication lines logically identified as paths 0 to N, and including changing  
3 (n) according to a repeating pattern beginning with (n) equal to 0 and increasing to (n)  
4 equal to N, and then decreasing to (n) equal to 0.

1 44. (Currently Amended) The method of claim 37, wherein performing the  
2 maintenance operation includes sending a calibration signal from a source on the  
3 communication line (n), the calibration signal comprising a signal pattern adapted for  
4 calibration of receive clock signals.

1 45. (Currently Amended) The method of claim 37, wherein performing the  
2 maintenance operation includes sending a calibration signal from a source on the  
3 communication line (n), the calibration signal comprising a pseudo random signal pattern  
4 adapted for calibration of receive clock signals.

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1 46. (Original) The method of claim 37, further including providing a source  
2 synchronous clock.

1 47. (Original) A signal interface, comprising:  
2 a set of signal lines;  
3 a set of receivers coupled to respective signal lines in the set of signal lines;  
4 a bus comprising a set of bus lines;  
5 a line maintenance circuit; and  
6 a switch coupled to the set of receivers, to the bus and to the line maintenance  
7 circuit, and control logic for the switch, which selectively routes signals in parallel from  
8 receivers in the set of receivers to bus lines in the set of bus lines and to the line  
9 maintenance circuit, where the receiver in the set of receivers routed to the line  
10 maintenance circuit is changed according to a pattern to selectively maintain signal paths  
11 over said set of signal lines without interrupting data flow from the set of receivers from  
12 the set of signal lines.

1 48. (Currently Amended) A transmission circuit on an integrated circuit, comprising:  
2 a line maintenance circuit to output a line maintenance signal;  
3 a set of transmitters coupled to receive a first set of signals and the line  
4 maintenance signal, and to output a second set of signals, wherein the second set of  
5 signals includes the first set of signals and the maintenance signal; and  
6 a switch coupled to the set of transmitters and a control logic for the switch, to  
7 selectively route the first set of signals and the line maintenance signal in parallel to the  
8 set of transmitters, where the transmitter in the set of transmitters routed to [by] the line  
9 maintenance circuit is changed according to a pattern to selectively maintain the second  
10 set of signals from the set of transmitters and to permit the maintenance signal to be used  
11 as a calibration signal, the transmitter in the set of transmitters routed to the line  
12 maintenance circuit is changed without interruption of transmission of the first set of  
13 signals.

1 49. (Currently Amended) A receiver circuit on an integrated circuit, comprising:

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2 means for receiving a first set of signals and a line maintenance signal, and to  
3 output a second set of signals;  
4 means for calibrating the means for receiving without interrupting the outputting  
5 of the second set of signals, the means for calibrating coupled to receive the line  
6 maintenance signal;  
7 means for routing the first set of signals and the line maintenance signal in  
8 parallel from the means for receiving, wherein the routing changes according to a pattern  
9 to selectively maintain the second set of signals and to permit the maintenance signal to  
10 be used as a maintenance signal for maintaining different portions of the means for  
11 receiving.

1 50. (New) A signal interface, comprising:  
2 a set of signal lines having  $N+1$  signal lines, where  $N$  is an integer;  
3  $N+1$  receivers coupled to respective signal lines in the set of signal lines  
4 establishing a set of  $N+1$  signal paths with the set of signal lines;  
5 an  $N$  line bus;  
6 a line maintenance circuit; and  
7 a switch in the  $N+1$  signal paths, and control logic for the switch, which  
8 selectively routes  $N$  signal paths in the set to the  $N$  line bus and signal path (n) in the set  
9 to the line maintenance circuit, where (n) is changed according to a pattern to selectively  
10 maintain signal paths in the set of  $N+1$  signal paths while enabling data flow on  $N$  signal  
11 paths in the set to the  $N$  line bus; wherein the line maintenance circuit performs  
12 calibration of the receiver coupled to signal path (n) routed to the line maintenance  
13 circuit, independent of the data flow on the  $N$  line bus.

1 51. (New) A signal interface, comprising:  
2 an  $N$  line bus;  
3 a set of signal lines having  $N+1$  signal lines, where  $N$  is an integer;  
4  $N+1$  transmitters coupled to respective signal lines in the set of signal lines  
5 establishing a set of  $N+1$  signal paths with the set of signal lines;  
6 a line maintenance circuit; and

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7 a switch in the N+1 signal paths, and control logic for the switch, which  
8 selectively routes N signal paths in the set from the N line bus to N signal lines in the set  
9 of signal lines, and routes signal path (n) in the set from the line maintenance circuit to  
10 signal line (n) in the set of signal lines, where (n) is changed according to a pattern to  
11 selectively perform maintenance on signal paths in the set of N+1 signal paths while  
12 enabling data flow on N signal paths in the set from the N line bus, independent of the  
13 data flow on the N line bus.

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